IVV PROCESS FOR AIRBORNE RADAR SOFTWARE - A CASE STUDY

Shayistha Banu A, JB Singh, Jithesh V, Justin Sagayaraj M
Electronics and Radar Development Establishment, C.V. Raman Nagar, Bengaluru, India

Abstract

Airborne Radars realize most of the operational and functional requirements through software. Airborne Radar Software in mission critical systems is a determinant of the success or failure of the mission. Software is mission critical in the sense failure or malfunction could result in failure of the mission, degraded performance or incomplete mission objectives. The objective of this paper is to demonstrate how DO-178B process helps to verify and validate radar functions that are captured in software from conceptualization to implementation and deployment through a case study.

1. Introduction

The software IV&V process determines whether the development of radar software confirms to its requirements and the software is airworthiness certified. The IV&V activities include analysis, evaluation, review, inspection, assessment and Testing of software products and software processes to ensure that the system requirements allocated to software are implemented correctly, completely and the requirements are consistent and testable.

DO-178B Guidelines are to be adhered to and objectives to be satisfied by airborne software to certify for airworthiness. The guidelines specify the rigour required in software development and assurance according to the criticality of software. The compliance to the DO-178B guidelines is verified by a Software Verification and Validation Team. The Verification and Validation process consists of Reviews, Analysis and Testing for verifying the compliance to DO-178B.

V&V can be an independent team, embedded in the development Team, embedded in the development team QA Group or embedded in the User Group.

The sections below describe the V&V Objectives, Process, Inputs for V&V at each phase of SDLC and the Outputs generated by V&V at end of each SDLC phase.

2. V&V Objectives

Independent V&V results in detailed analysis and test of software requirements and early detection of critical system and software errors. Software V&V determines that the software performs its intended functions correctly. And it ensures that the software performs no unintended functions. It measures and assesses the quality and reliability of the software. Software V&V also analyses and tests the software on how it interfaces with system elements and how it influences the performance or reacts to stimuli from system elements.

3. V&V Process

The core Sub-systems of Radar possesses the capabilities of Target Detection, Resource Allocation, Multi-Target Tracking and Display. As 60% to 70% of Radar System functionalities are implemented in Software they are verified and validated through DO-178B process Objectives. The airborne radar software is verified and validated for correctness of algorithms, traceability and timing analysis. Rigorous testing is carried out for checking resource sharing, redundancy, fault tolerance, failure detection, timing and scheduling requirements.

V&V main objective is to determine whether the software satisfies the critical system requirements. And hence the V&V tasks are oriented towards algorithm analysis, control and data flow analysis and comprehensive testing.

The IV&V activities are carried out throughout the software development lifecycle after each phase of SDLC. The following diagram describes the timing of IV&V activities;

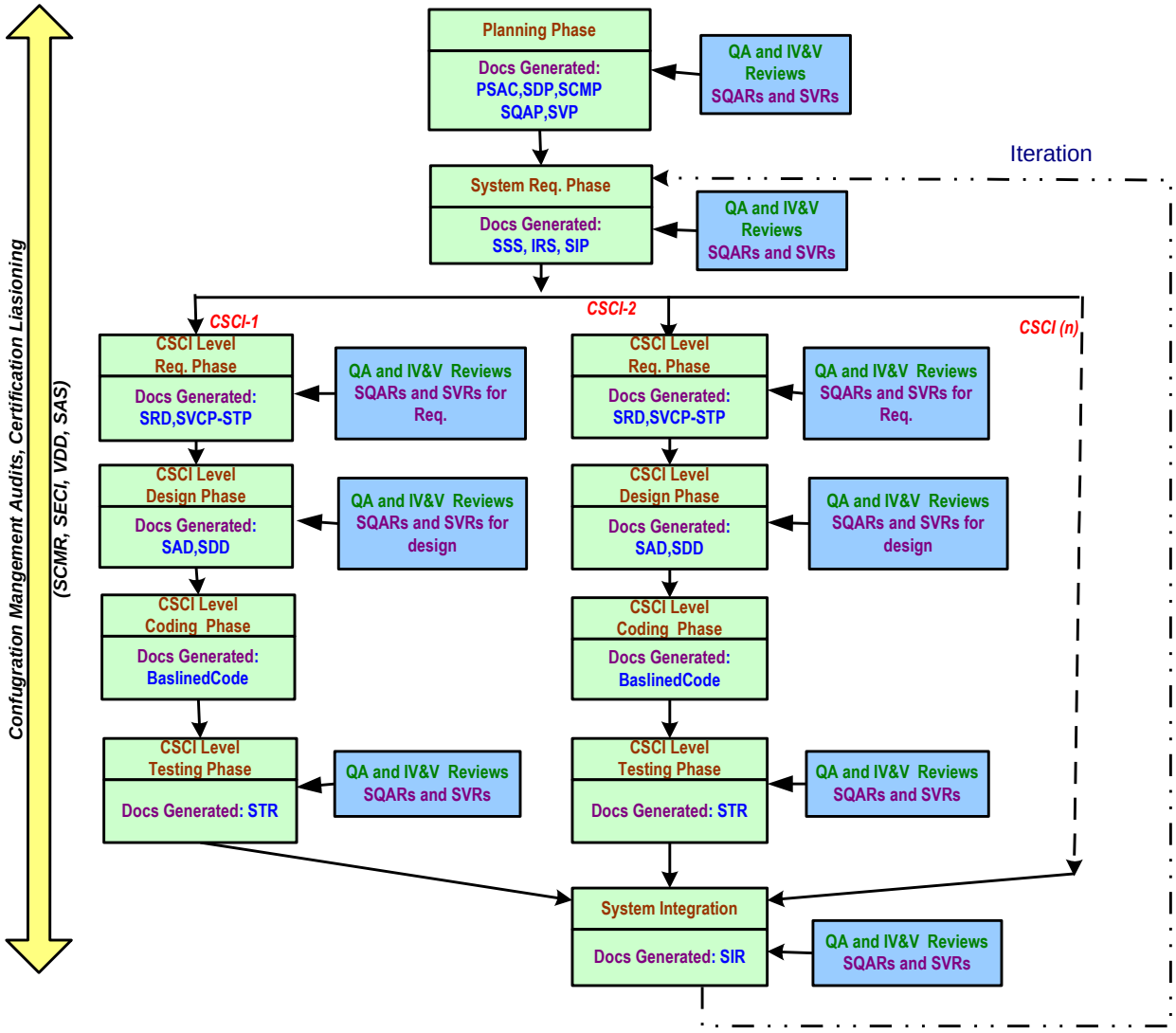

Figure 1: Schedule of IV&V Activities (DO-187B Level D)

As per the SDLC provided in Figure 1, the outputs of planning phase Plan for Software Aspects of Certification (PSAC) and Software Verification Plan (SVP) are subjected to IVV Review and SVRs are generated. During the System Software Requirements Phase, System Sub-system Specification (SSS), Interface Requirements Specification (IRS) are subjected to IVV review and SVRs are generated. In Software Requirements phase the Software Requirements Data (SRD) of each Sub-system and respective Software Test Plans are subjected to IVV Review and SVRs are generated. In Software Design Phase the Software Architectural Design of all Sub-systems are subjected to IVV review and SVRs are generated. Except for DO-178B Level D, for all Safety levels from C to A the Software Detailed Design (SDD), Module level Integration Test plans (ITP) and Unit Test Plans (UTP) are subjected to IVV review and SVRs are generated. During the Coding Phase the Source Code is subjected to Static and Dynamic Testing and Coverage analysis Report is generated and subjected to IVV review. During Integration Testing stage the software integration report (SIR) is subjected to IVV reviews and SVRs generated.

Results of IV&V performed on one of the airborne radar software of LRDE are taken as a case study here and results at each IV&V phase are provided.

3.1 *Verification of Outputs of Software Requirement Process*

During the Software Requirements Review, IV&V performs the following;

1. System requirements allocated to the software are defined and they do not contain inconsistencies.
2. States & Modes are captured correctly in High Level Requirements (HLR) in line with system requirements.
3. Functional, performance and safety requirements are developed & traceable to system requirements.
4. Derived requirements and the reason for their existence are correctly defined.
5. Each HLR requirement is accurate, testable and is stated in quantitative terms with tolerances and no conflicts exist between high level requirements & the hardware/software features of the target computer, especially system response times, bandwidth and the input/output hardware.

IV&V also ensures the accuracy and behaviour of the proposed algorithms by performing Algorithm Verification ((Ref: IEEE Software verification Process Standard IEEE-1012.1998 Appendix G.) with following steps:

a. Re-derive equations from basic principles and theories if feasible
b. Compare with Established references and historic data.
c. Perform verifications of Simulation models and programs.

d. Perform verification on verification of Algorithm verification report submitted.
e. The verified Simulation models will be used for verifying algorithm output during HLR testing.
f. This objective is met by review at HLR requirement process and finally evidenced during HLR testing.

Some of the algorithms verified using Matlab models in various radar sub-systems are listed below:

a. Signal processing algorithms - CFAR, FFT
b. Data processing algorithms - IMM Filter
c. Data Association algorithms - Munkres etc...

The figure 2 below gives the details on IV&V reviews carried out on System Software Requirements, Interface Requirements and Sub-system software Requirements of Radar.

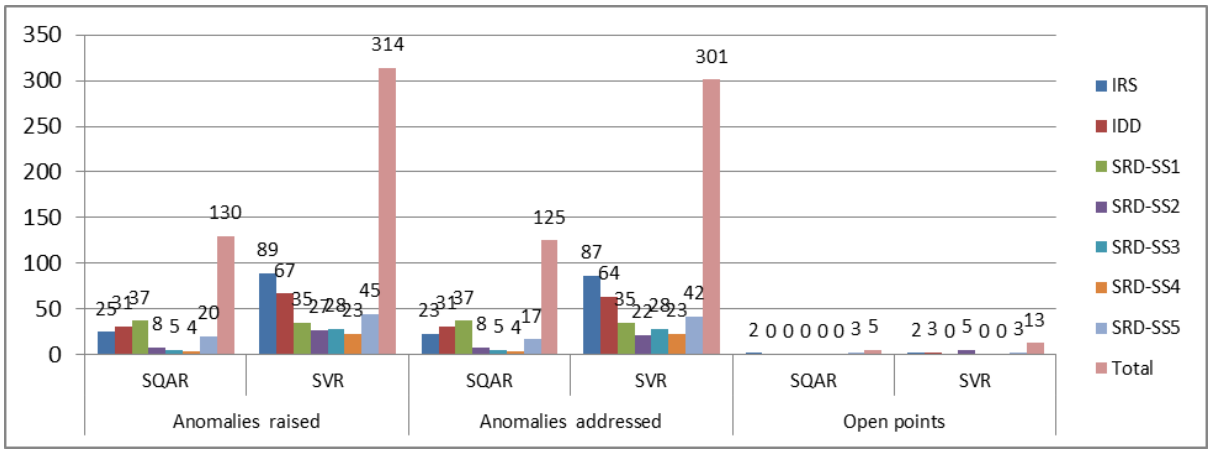

Figure 2: Software Requirements Review and Results

3.2 *Verification of Outputs of Software Design Process*

During the Software Design Review IV&V verifies the following;

1. Verify bidirectional traceability between HLR and Architecture.
2. Verify that the diagrams in architectural design document should bring out Control Flow, Data Flow, Internal sequence diagram and activity diagram with in software.
3. Projected Call graph at design stage is also required.
4. Safety Requirement related Architectural components should be available in SAD (Watch dog timers, etc.)
5. Verify Control and Data flow integrity between components of software architecture.
6. Verify Architecture design for conformance with performance and resource capabilities of target hardware.
7. Verify Interrupt service routine details, IPC & Synchronization Mechanisms periodicity of tasks, execution Timing constraints imposed by system requirements and target hardware for each component of software at architecture level.
8. Perform Schedulability Analysis of tasks and interrupt service routines.

9. Verify that the cyclic calls (recursion) are avoided.
10. Verify exponential complexity algorithms are restricted by tolerable finite bound.
11. The architecture should capture internal interfaces between software components, IPC mechanisms, task priorities, etc.
12. Verify the partitioning details where applicable.

The figure 3 below gives the details of IV&V reviews carried out on sub-system software architectural design of Radar.

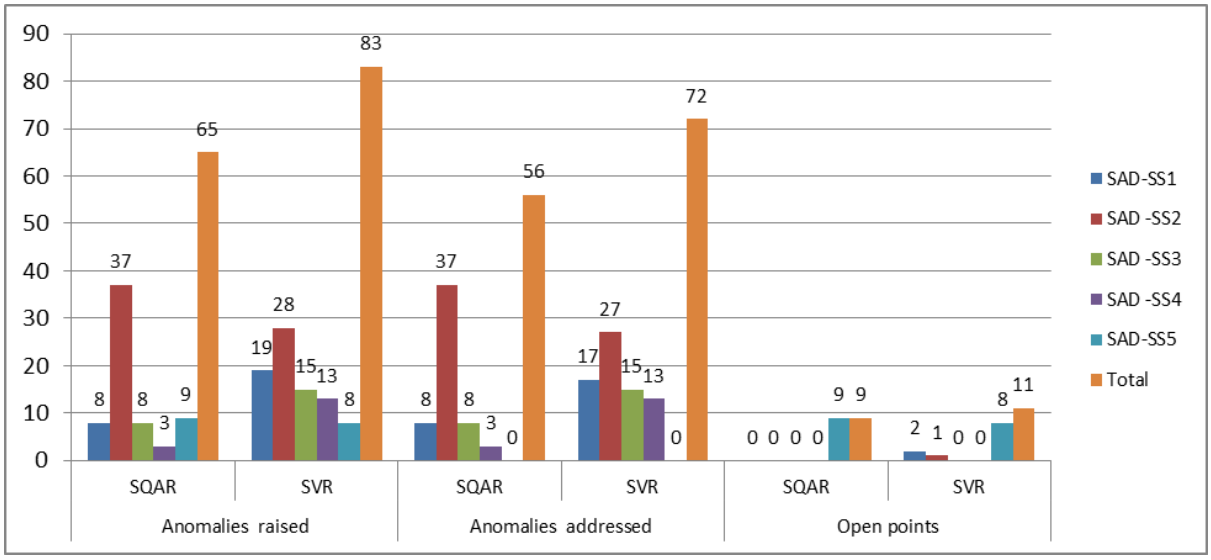

Figure 3: Software Design reviews and results

3.3 *Testing of Outputs of Software Coding and Integration Process*

During Testing of outputs of Software Coding and Integration Process IV&V validates the following;

1. Source code is accurate & complete wrt Low Level Requirements (LLRs).
2. No source code implements undocumented functions.
3. Ensure that the source code matches the data flow and control follow defined in the s/w architecture.
4. Ensure that Code does not contain Statements that cannot be verified.
5. Ensure that Code does not contain the structure that cannot be verified
6. Ensure that Code does not have to be altered to test it.
7. Software Coding Standards are followed.
8. Ensure that the complexity restrictions and code constraints are followed:
    a. Complexity includes coupling between s/w components, nesting Level, logical and numerical expressions.
9. Ensure that source code is traceable to LLR.
10. Determine the correctness and consistency of the Source Code, including stack usage, fixed point arithmetic overflow and resolution, resource contention, worst-case execution timing, exception handling, use of uninitialized variables or constants, unused variables or constants, and data corruption due to task or interrupt conflicts.

11. Some of the objectives such as worst-case execution timing may be demonstrated during unit test report.
12. Check for complier warnings
    a. Incorrect h/w addresses
    b. Memory overlaps
    c. Missing s/w components

Static and Dynamic testing tools are used for Source Code Review and Verification. Figure 4 below gives details of IV&V Reviews carried on Sub-system Software Test plans and procedures.

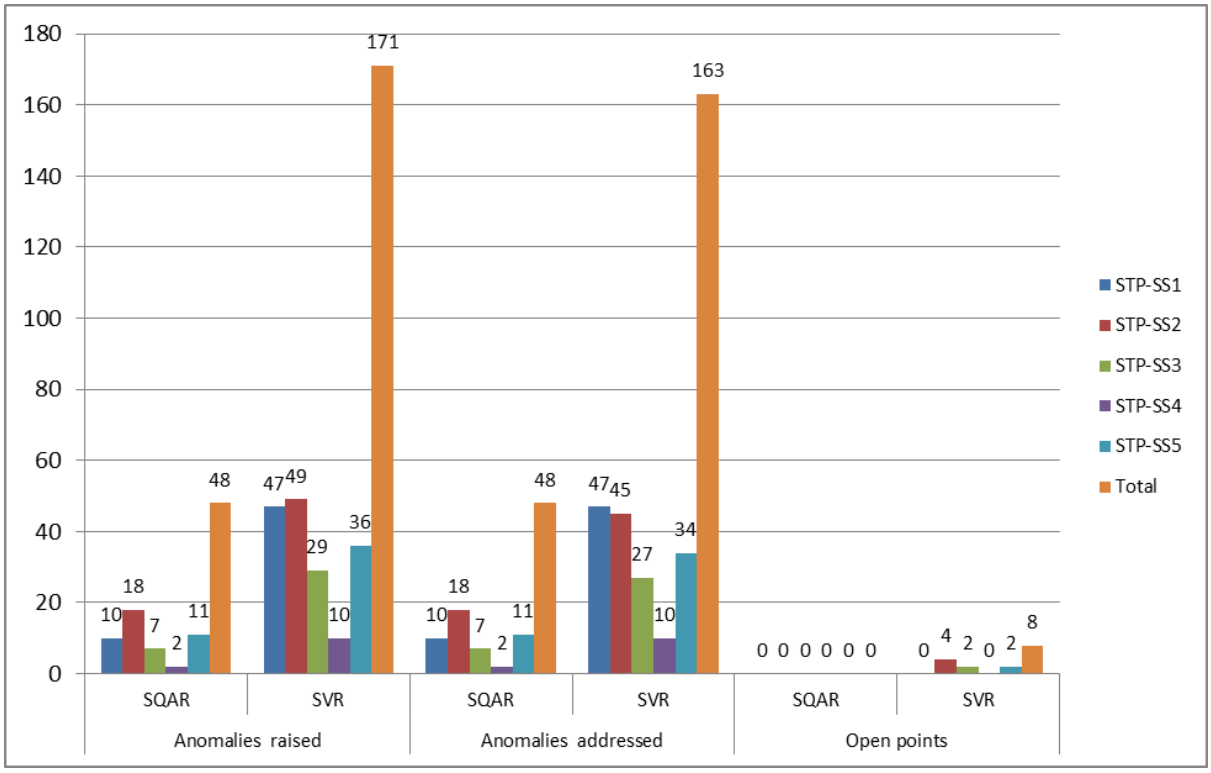

Figure 4: Software Testing and Results

3.4 *Testing of Outputs of Integration Process*

During Testing of outputs of Integration Process IV&V validates the following;

1. Test Cases are developed from software requirements and are traceable to software requirements
2. Test cases are developed to include normal and robust cases from requirements
3. TCs are traceable.
4. Tests are performed in the integrated target computer environment
5. Requirement based h/w & s/w integration test are performed on the target h/w to ensure the compatibility.

Figure 5 below gives details of IV&V Reviews carried on Software Integration Plan and procedures of Radar Sub-system.

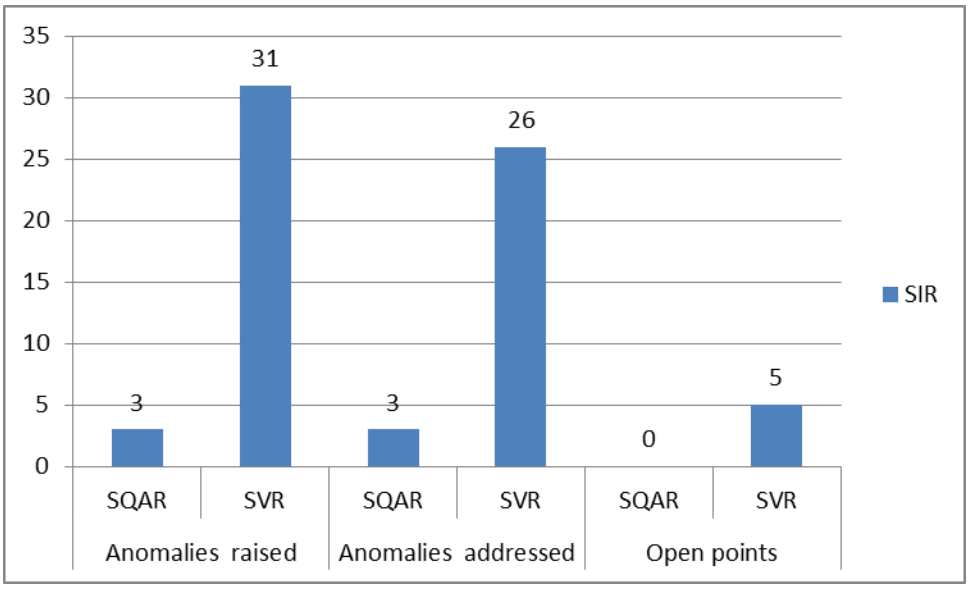

Figure 5: Software Integration Testing and Results

3.5 Verification of Verification Process Results

During Verification of verification process results IV&V validates the following;

1. Test Cases are correctly developed into test procedures
2. Test procedures include expected results.
3. Test results are correct and any discrepancy between actual result and expected result are explained.
4. Ensure that Test Case exist for each requirement
5. Confirm that the test cases used to achieve structural coverage are traceable to requirements.
6. Perform structural coverage analysis on the source code
7. Analyse structural coverage results collected during requirement based testing to find out which code structure (decision) are not exercised.
8. Additional test / verification cases produced to provide structural coverage.
9. Perform coverage analysis resolution (ref: 6.4.4.3 of DO Table 178B standard)
10. Confirm that the requirement based testing has exercised the data and control coupling between code components. (Ref: Cast-19).
11. Demonstrate RBT either at Software testing or module integration testing covered data and control coupling are exercised.
12. The testing should cover internal interfaces between processes, tasks, and modules
13. Test should include control coupling issues such as scheduling, IPC synchronization mechanism, and execution timing constraints on algorithms etc.

Figure 6 below gives the details of IV&V Code review and verification carried out on Radar Sub-system Software.

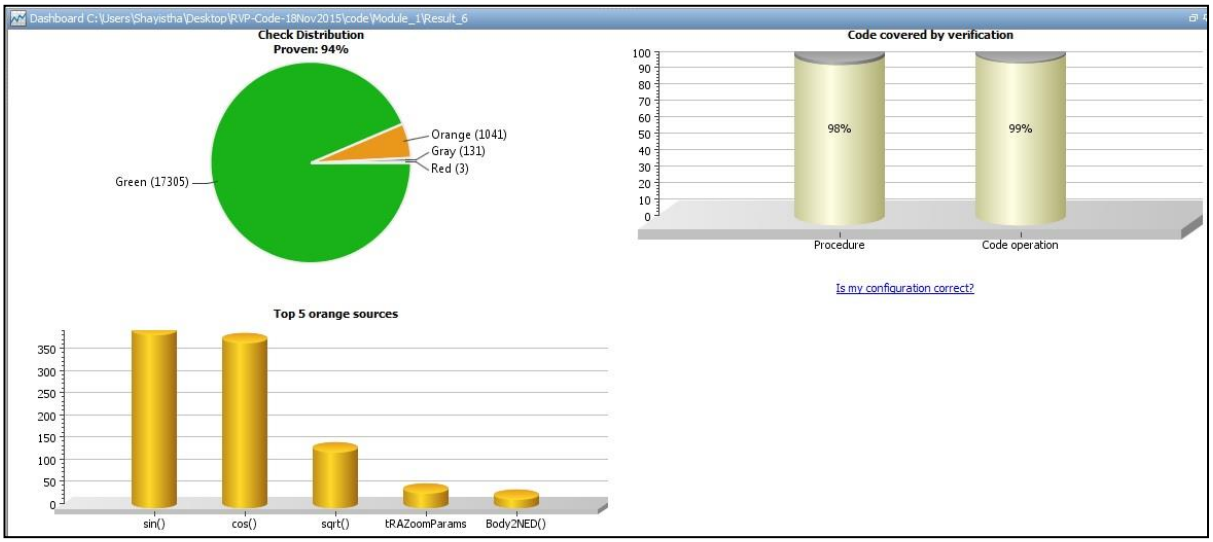

Figure 6: Source Code Verification and Results (Polyspace Code Prover – snap shot)

The Lifecycle data generated throughout the SDLC and the Outputs of IV&V are produced to the certification agency during the Stages of Involvement reviews (SOI) as evidences of compliance to DO-178B process and approval is obtained.

4. Conclusion

As 60% to 70% of Radar System functionalities are implemented in Software they are verified and validated through DO-178B process Objectives. Adherence to DO-178B ensures that there are no requirements which have not been tested. There exist no known errors in the software which may result in failure or degraded performance of the radar system.

References

1. IEEE - Software verification Process Standard IEEE-1012.1998 Appendix G
2. RTCA DO-178B Software Considerations in airborne systems and equipment certification
3. DO-178B, CAST Papers
4. LRDE, DO-178B Product Review Checklists.